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|--|-------------------------|--|------|--|-------------------------------|-----------------|--|
| | | | | | Application Number 10/590,613 | | |
| INFORMATION DISCLOSURE | | | | | Filing Date | August 24, 2006 | |
| STATEMENT BY APPLICANT (use as many sheets as necessary) | | | | | First Named Inventor: | Andrey Efimov | |
| | | | | | Art Unit | 2112 | |
| | | | | | Examiner Name | Enam Ahmed | |
| Sheet | 1 | | of 1 | | Attorney Docket Number | 42P23458 | |
| NON PATENT LITERATURE DOCUMENTS | | | | | | | |
| Examiner Initials* | Cite No ¹ | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published | | | | | |
| | 1. | IEEE Standard 802.3an, approved on June 8, 2006, published September 1, 2006, 19 pages. | | | | | |
| | 2. | TANNER, R., "A Recursive Approach to Low Complexity Codes", IEEE Trans. Inform. Theory, 1981, pp. 533-547, Vol. IT-42. | | | | | |
| | 3. | SCHERSON, I. et al., "Bit-Parallel Arithmetic in a Massively-Parallel Associative Processor", IEEE Transactions on Computers, October 1992, pp. 1201-1210, Vol. 41, No. 10. | | | | | |
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